REMARKS

Status of the Claims

Claims 1-20 remain pending.

Rejections Under 35 USC § 103

To make an obviousness rejection, the examiner must establish a prima facie case. See MPEP 2142.

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

MPEP 2142.

The examiner rejected claims 1-6, 8-9, 11-14 and 16-20 under 35 USC § 103 as being anticipated by U.S. Patent No. 5,949,691 ("Kurosaka") in view of U.S. Patent No. 6,141,630 ("McNamara"). The examiner further rejected claims 7, 10 and 15 under Kurosaka in view of McNamara and U.S. Patent No. 5,684,808 ("Valind"). Applicant respectfully traverses these rejections.

Claim 1 recites in part: "a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter a "test pattern"). The examiner cites Kurosaka's teaching of an intermediate format data file 106 as anticipating a pattern profile that represents a test pattern. However, Kurosaka does not here or elsewhere teach or suggest the quoted element. To the contrary, Kurosaka teaches "The data file 106 in the intermediate format ... is provided ... to store detailed circuit information". Col. 7, lines 6-9. Kurosaka uses this file to store circuit information for two circuits that he wishes to compare using a point-detection

algorithm. Col. 7, lines 12-16. No sequence of input signal vectors is represented by data file 106.

McNamara teaches a test generator that constructs a set of test vectors from a circuit design coded in a circuit design language. Col. 3, lines 22-43. The test generator interprets the circuit design as a series of blocks connected by transition arcs to form a state diagram, and constructs a first set of test vectors to cause each block to be visited and each transition arc to be taken. A second set of test vectors is also constructed to ensure user-selected transition paths are taken. Col. 4, lines 28-37. As with Kurosaka, the data structures represent the circuit design, and not a test pattern. The examiner cites, and applicant finds, no teaching or suggestion of a test pattern profile in McNamara.

Valind teaches an automatic test pattern generator 56 that operates on a detailed circuit description 54 to generate test patterns. Fig. 4. The test pattern generator uses logic cone tracing and partitioning of the circuit logic to generate scan vectors that will detect stuck-at-1 and stuck-at-0 faults. Col. 9, lines 15-50. The examiner cites the detailed circuit description 54 as anticipating applicant's claimed test pattern profile. However, as with Kurosaka and McNamara, the detailed circuit description and derivative data structures are used to represent the circuit design, and not a test pattern.

Independent claims 11 and 17 also recite test pattern profiles as required elements. Applicant respectfully submits that independent claims 1, 11 and 17, along with their dependent claims, are allowable over the cited art for at least the reasons given above.

Conclusion

In the course of the foregoing discussions, applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

Applicant submits that this response constitutes a complete response to all of the issues raised in the Office Action dated June 20, 2002. Applicant has responded to the various rejections under 35 U.S.C. § 102(e) and 103(a). In view of the foregoing amendments and remarks, applicant submits that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. If any fees are inadvertently omitted or if any additional fees are required or have been overpaid, please appropriately charge or credit those fees to LSI Logic Deposit Account Number 12-2252/P-3270/DJK.

Respectfully submitted,

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